Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **GND**
2. **ENABLE**
3. **INPUT**
4. **INPUT**
5. **INPUT**
6. **INPUT**
7. **OUTPUT**
8. **OUTPUT**
9. **OUTPUT**
10. **OUTPUT**
11. **ADJUST**

**.143”**

**7**

**8**

**9**

**10**

**11**

**6**

**5**

**4**

**3**

**2**

**1**

**MIC29500-AC**

**MASK**

**REF**

**.161”**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: .004 x .004”**

**Backside Potential: GND**

**Mask Ref: MIC29500-AC**

**APPROVED BY: DK DIE SIZE .143” X .161” DATE: 6/13/23**

**MFG: MICREL THICKNESS .014” P/N: MIC29502**

**DG 10.1.2**

#### Rev B, 7/1